Triple single-pole double-throw analog switch Rev. 12 — 25 March 2016

Product data sheet

1. General description

The HEF4053B is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input (\overline{E}). A HIGH on \overline{E} causes all switches into the high-impedance OFF-state, independent of Sn.

 V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (Sn and \overline{E}). The V_{DD} to V_{SS} range is 3 V to 15 V. The analog inputs/outputs (nY0, nY1 and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1.Ordering information

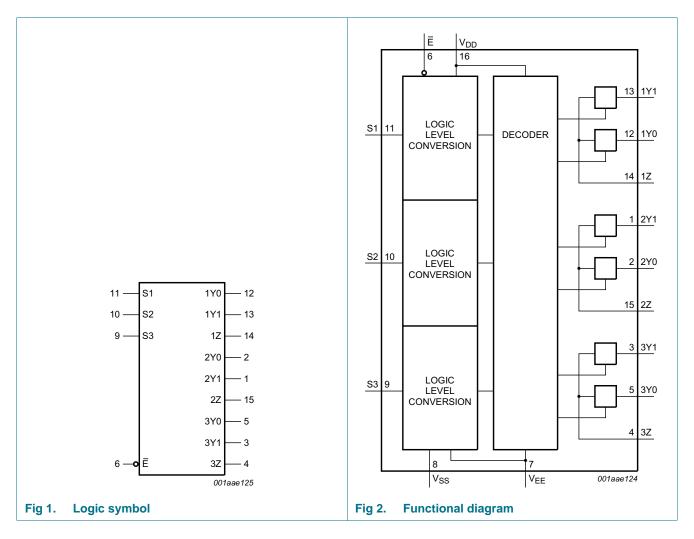
All types operate from -40 ℃ to +125 ℃.

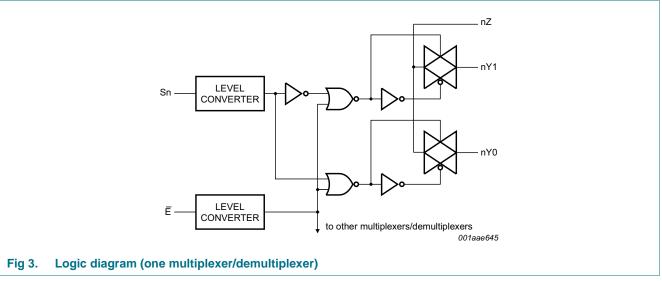
Type number	Package	Package					
	Name	Description	Version				
HEF4053BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1				
HEF4053BTT	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1				

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5. Functional diagram

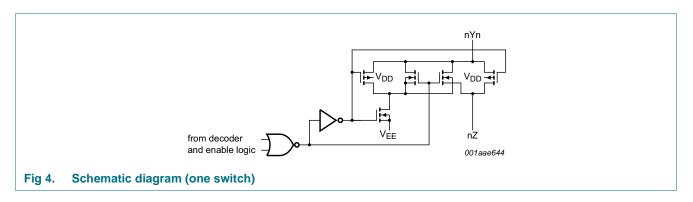




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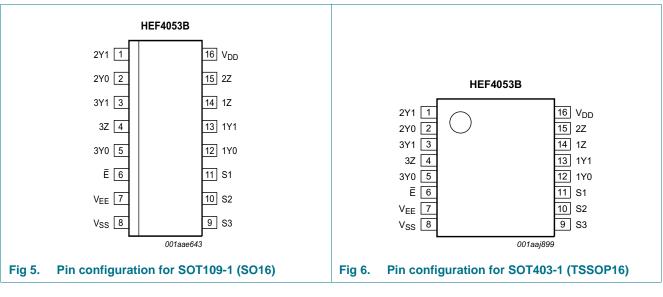
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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2.Pin description

Symbol	Pin	Description
Ē	6	enable input (active LOW)
V _{EE}	7	supply voltage
V _{SS}	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	independent output or input
V _{DD}	16	supply voltage

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7. Functional description

Table 3.Function table [1]

Inputs	Channel on	
Ē	Sn	
L	L	nY0 to nZ
L	Н	nY1 to nZ
Н	X	switches OFF

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 V$ (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DD}	supply voltage			-0.5	+18	V
V _{EE}	supply voltage	referenced to V _{DD}	[1]	-18	+0.5	V
I _{IK}	input clamping current	pins Sn and \overline{E} ; V _I < -0.5 V or V _I > V _{DD} + 0.5 V		-	±10	mA
VI	input voltage			-0.5	V _{DD} + 0.5	V
I _{I/O}	input/output current			-	±10	mA
I _{DD}	supply current			-	50	mA
T _{stg}	storage temperature			-65	+150	°C
T _{amb}	ambient temperature			-40	+125	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \text{ to } +125 \ ^{\circ}C$				
		SO16 package	[2]	-	500	mW
		TSSOP16 package	[2]	-	500	mW
Р	power dissipation	per output		-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

For SO16 package: Ptot derates linearly with 8 mW/K above 70 °C.
 For TSSOP16 package: Ptot derates linearly with 5.5 mW/K above 60 °C.

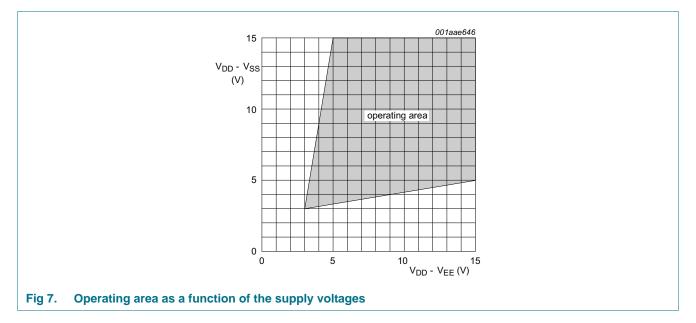
9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DD}	supply voltage	see Figure 7	3	-	15	V
VI	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall	V _{DD} = 5 V	-	-	3.75	μs/V
	rate	V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

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10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = V_{EE} = 0 V$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	–40 °C	T _{amb} =	25 °C	T _{amb} =	85 °C	T _{amb} =	125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	Z port; all channels OFF; see <u>Figure 8</u>	15 V	-	-	-	1000	-	-	-	-	nA
		Y port; per channel; see <u>Figure 9</u>	15 V	-	-	-	200	-	-	-	-	nA
I _{DD}	supply current	I _O = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
CI	input capacitance	Sn, \overline{E} inputs	-	-	-	-	7.5	-	-	-	-	pF

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10.1 Test circuits

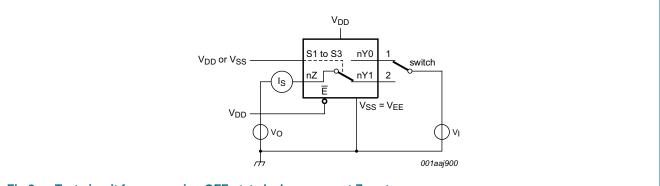
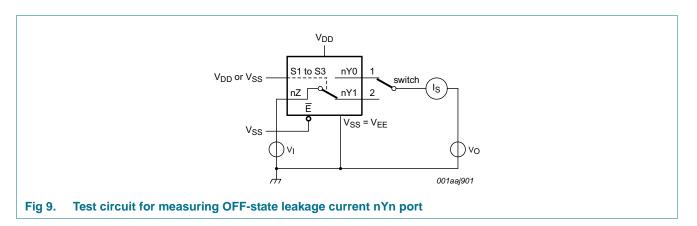


Fig 8. Test circuit for measuring OFF-state leakage current Z port



10.2 ON resistance

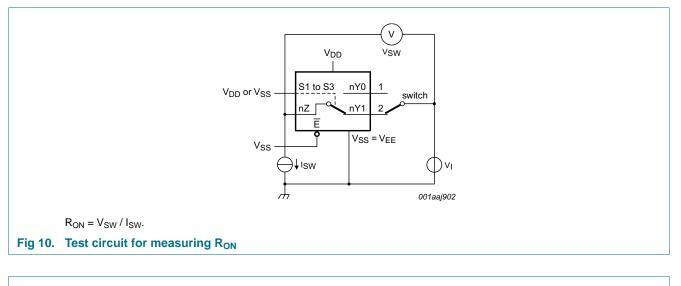
Table 7. ON resistance

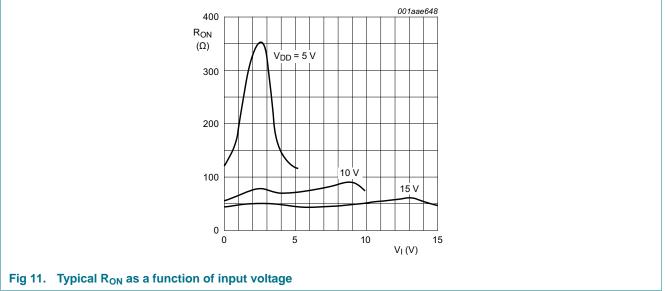
 $T_{amb}=25~^\circ\!\mathrm{C};\,I_{SW}=200~\mu\mathrm{A};\,V_{SS}=V_{EE}=0~V.$

Symbol	Parameter	Conditions	$V_{DD} - V_{EE}$	Тур	Max	Unit
R _{ON(peak)}	ON resistance (peak)	$V_I = 0 V \text{ to } V_{DD} - V_{EE};$	5 V	350	2500	Ω
		see <u>Figure 10</u> and <u>Figure 11</u>	10 V	80	245	Ω
			15 V	60	175	Ω
R _{ON(rail)}	ON resistance (rail)	$V_I = 0 V$; see <u>Figure 10</u> and <u>Figure 11</u>	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		$V_{I} = V_{DD} - V_{EE};$	5 V	120	365	Ω
		see Figure 10 and Figure 11	10 V	65	200	Ω
			15 V	50	155	Ω
ΔR_{ON}	ON resistance mismatch	esistance mismatch $V_{I} = 0 V$ to $V_{DD} - V_{EE}$; see Figure 10		25	-	Ω
betwe	between channels		10 V	10	-	Ω
			15 V	5	-	Ω

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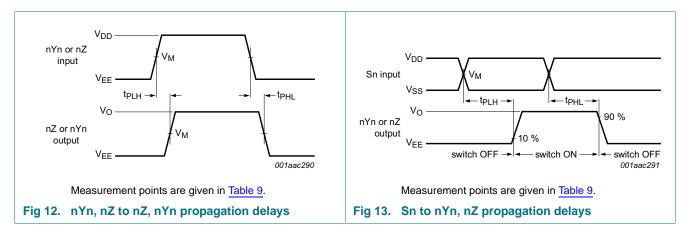
11. Dynamic characteristics

Table 8. Dynamic characteristics

 $T_{amb} = 25 \text{ °C}; V_{SS} = V_{EE} = 0 \text{ V}; \text{ for test circuit see } Figure 15.$

Symbol	Parameter	Conditions	V _{DD}	Тур	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nYn, nZ to nZ, nYn; see Figure 12	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Figure 13	5 V	200	400	ns
			10 V	85	170	ns
			15 V	65	130	ns
t _{PLH}	LOW to HIGH propagation delay	nYn, nZ to nZ, nYn; see Figure 12	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Figure 13	5 V	275	555	ns
			10 V	100	200	ns
			15 V	65	130	ns
t _{PHZ}	HIGH to OFF-state	E to nYn, nZ; see Figure 14	5 V	200	400	ns
	propagation delay		10 V	115	230	ns
			15 V	110	220	ns
t _{PZH}	OFF-state to HIGH	E to nYn, nZ; see Figure 14	5 V	260	525	ns
	propagation delay		10 V	95	190	ns
			15 V	65	130	ns
t _{PLZ}	LOW to OFF-state	Ē to nYn, nZ; see <u>Figure 14</u>	5 V	200	400	ns
	propagation delay		10 V	120	245	ns
			15 V	110	215	ns
t _{PZL}	OFF-state to LOW	Ē to nYn, nZ; see <u>Figure 14</u>	5 V	280	565	ns
	propagation delay		10 V	105	205	ns
			15 V	70	140	ns

11.1 Waveforms and test circuit



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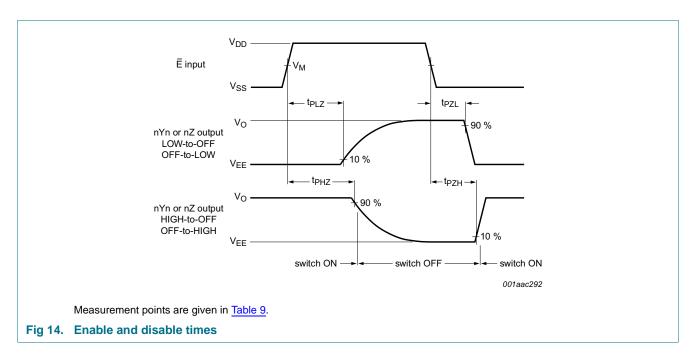


Table 9.Measurement points

Supply voltage	Input	Output
V _{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}

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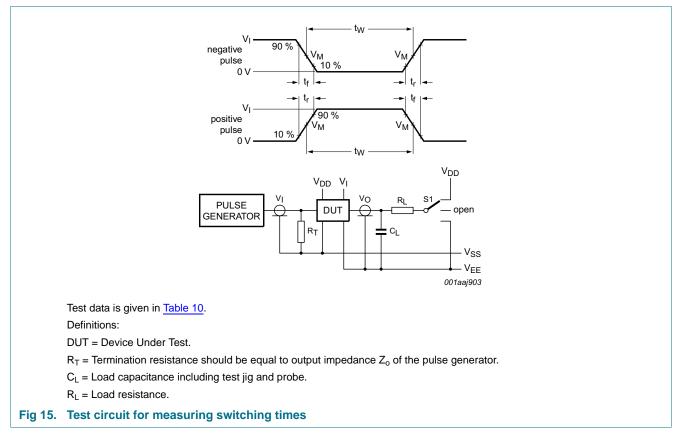


Table 10. Test data

Input			Load		S1 position	l				
nYn, nZ	Sn and \overline{E}	t _r , t _f	V _M	CL	RL	t _{PHL} [1]	t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	≤ 20 ns	$0.5V_{DD}$	50 pF	10 kΩ	$V_{\text{DD}} \text{ or } V_{\text{EE}}$	V _{EE}	V _{EE}	V _{DD}	V_{EE}

[1] For nYn to nZ or nZ to nYn propagation delays use V_{EE}. For Sn to nYn or nZ propagation delays use V_{DD}.

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11.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

 $V_{\text{SS}} = V_{\text{EE}} = 0$ V; $T_{\text{amb}} = 25$ °C.

Symbol	Parameter	Conditions	V _{DD}		Тур	Max	Unit
THD	total harmonic distortion	see Figure 16; $R_L = 10 \text{ k}\Omega$; $C_L = 15 \text{ pF}$;	5 V	<u>[1]</u>	0.25	-	%
		channel ON; V _I = 0.5V _{DD} (p-p); f _i = 1 kHz	10 V	<u>[1]</u>	0.04	-	%
		$i_j = 1$ Ki iz	15 V	<u>[1]</u>	0.04	-	%
f _(-3dB)	-3 dB frequency response	$\frac{1}{2}$	5 V	<u>[1]</u>	13	-	MHz
			10 V	<u>[1]</u>	40	-	MHz
			15 V	<u>[1]</u>	70	-	MHz
α_{iso}	isolation (OFF-state)	see Figure 18; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ k}\Omega$; $C_L = 5 \text{ pF}$; channel OFF; $V_I = 0.5V_{DD} \text{ (p-p)}$	10 V	<u>[1]</u>	-50	-	dB
V _{ct}	crosstalk voltage	digital inputs to switch; see Figure 19; $\frac{R_L}{E} = 10 \text{ k}\Omega$; $C_L = 15 \text{ pF}$; E or Sn = V _{DD} (square-wave)	10 V		50	-	mV
Xtalk	crosstalk	between switches; see Figure 20; $f_i = 1 \text{ MHz}; R_L = 1 \text{ k}\Omega;$ $V_I = 0.5V_{DD} \text{ (p-p)}$	10 V	[1]	-50	-	dB

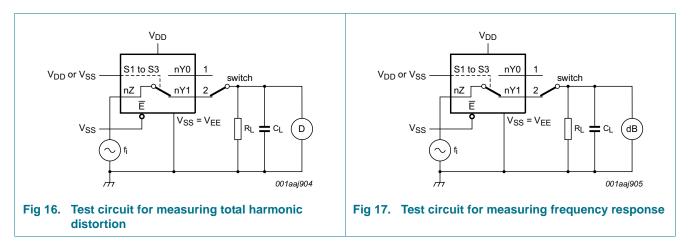
[1] f_i is biased at 0.5 V_{DD}; V_I = 0.5V_{DD} (p-p).

Table 12.Dynamic power dissipation PD

 P_D can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0$ V; $t_r = t_f \le 20$ ns; $T_{amb} = 25$ °C.

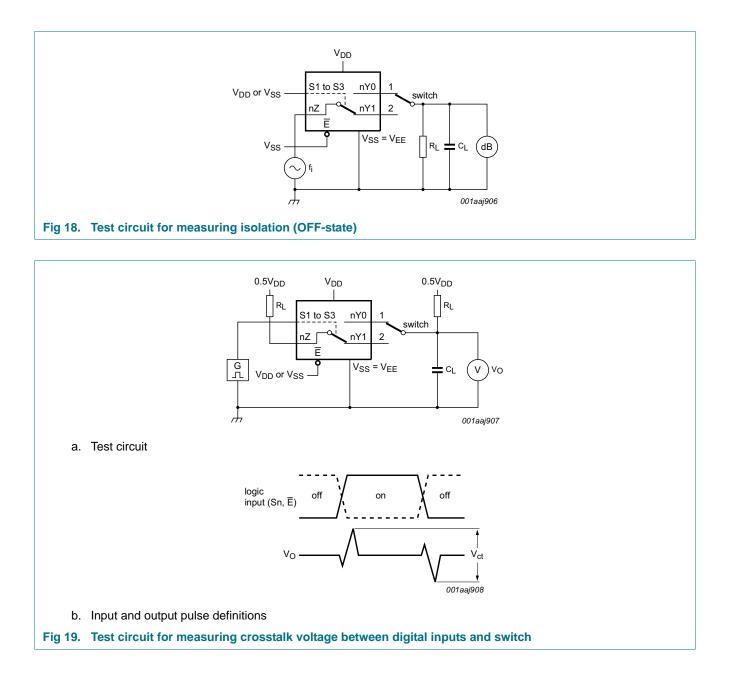
Symbol	Parameter	V _{DD}	Typical formula for P_D (μ W)	where:
PD	dynamic power	5 V	$P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_DD{}^2$	$f_i = input frequency in MHz;$
	dissipation	10 V	$P_{D} = 11500 \times f_{i} + \Sigma(f_{o} \times C_{L}) \times V_{DD}^{2}$	f _o = output frequency in MHz;
		15 V	$P_{D} = 29000 \times f_{i} + \Sigma (f_{o} \times C_{L}) \times V_{DD}^{2}$	C _L = output load capacitance in pF;
				V _{DD} = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

11.2.1 Test circuits



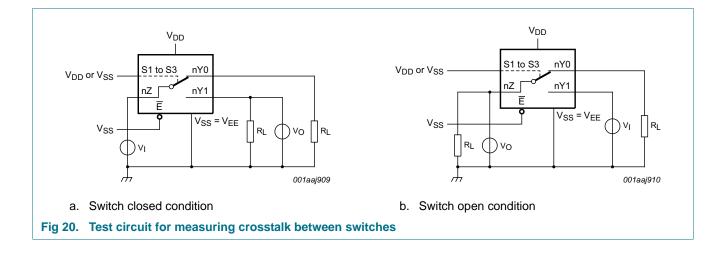
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12. Package outline

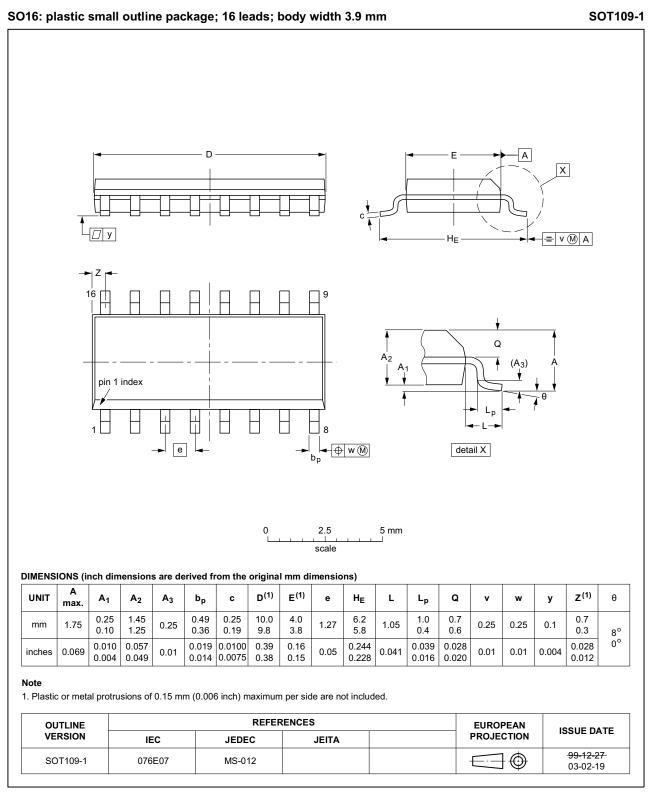


Fig 21. Package outline SOT109-1 (SO16)

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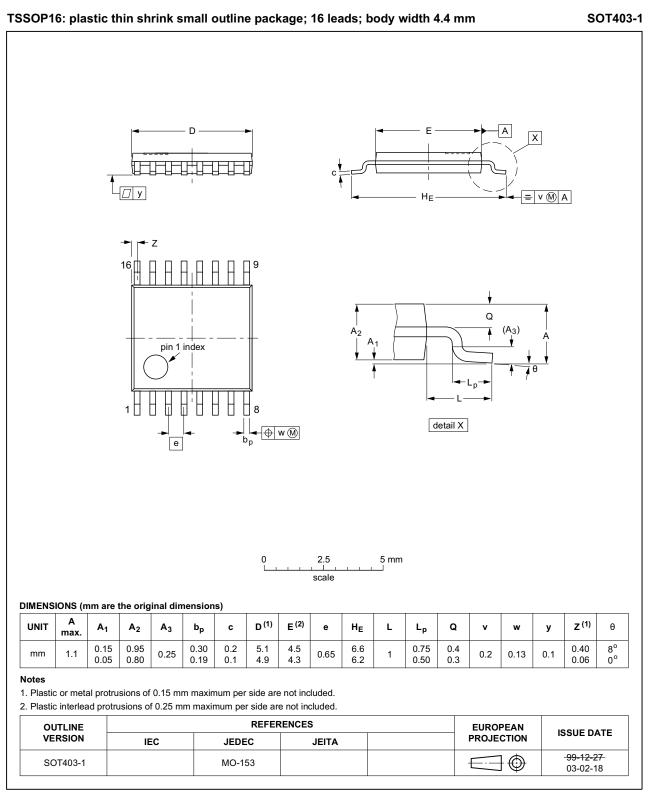


Fig 22. Package outline SOT403-1 (TSSOP16)

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13. Abbreviations

Table 13. Abbreviations		
Acronym	Description	
DUT	Device Under Test	

14. Revision history

Table 14. Revision history					
Document ID	Release date	Data sheet status	Change notice	Supersedes	
HEF4053B v.12	20160325	Product data sheet	-	HEF4053B v.11	
Modifications:	 Type number 	er HEF4053BP (SOT38-4) ren	noved.	·	
HEF4053B v.11	20140911	Product data sheet	-	HEF4053B v.10	
Modifications:	<u>Figure 19</u> : Test circuit modified				
HEF4053B v.10	20111117	Product data sheet	-	HEF4053B v.9	
Modifications:	 Legal pages 	updated.	·		
	 Changes in 	"General description", "Featu	res and benefits" and	"Applications".	
HEF4053B v.9	20100325	Product data sheet	-	HEF4053B v.8	
HEF4053B v.8	20100224	Product data sheet	-	HEF4053B v.7	
HEF4053B v.7	20091127	Product data sheet	-	HEF4053B v.6	
HEF4053B v.6	20090924	Product data sheet	-	HEF4053B v.5	
HEF4053B v.5	20090825	Product data sheet	-	HEF4053B v.4	
HEF4053B v.4	20090713	Product data sheet	-	HEF4053B_CNV v.3	
HEF4053B_CNV v.3	19950101	Product specification	-	HEF4053B_CNV v.2	
HEF4053B_CNV v.2	19950101	Product specification	-	-	

Table 14. Revision history

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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